Claims

1. An apparatus (1) for utilization with the synchronization of clock signals (CLK), comprising delay device (2) with a variably controllable delay time (t_{var}) into which a clock signal (CLK), or a signal obtained therefrom, is input, charged with the variably controllable delay time (t_{var}), and output as a delayed clock signal (DQS),

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a device (5) is provided for determining whether a clock edge (A') of the delayed clock signal (DQS) output by the delay device (2), or of a signal (FB) obtained therefrom, lies within a predetermined time window before a corresponding clock edge (A) of the clock signal (CLK), or of the signal obtained therefrom.

2. The apparatus (1) according to claim 1, wherein, if it is determined that the clock edge (A') of the delayed clock signal (DQS) output by said delay device (2), or of the signal (FB) obtained therefrom, lies within the predetermined time window before the corresponding clock edge (A) of the clock signal (CLK), or of the signal obtained therefrom, said device (5) sends a determination signal (SLOW) to said delay device (2).

3. The apparatus (1) according to claim 2, wherein said delay device (2) changes from a first to a second mode in reaction to said determination signal (SLOW).

4. The apparatus (1) according to any of the preceding claims, wherein, if said device (5) determines that the clock edge (A') of the delayed clock signal (DQS) output by said delay device (2), or of the signal (FB) obtained therefrom,

lies within the predetermined time window before the corresponding clock edge (A) of the clock signal (CLK), or of the signal obtained therefrom, the signal delay time (t_{var}) caused by said delay device (2) is decremented or incremented in smaller time steps than prior to the determination.

5. The apparatus (1) according to any of the preceding claims, wherein the duration (Δt) of the time window is chosen as a function of the frequency of the clock signal (CLK), in particular a delay device (13) provided in said determination device (5) is - for this purpose - correspondingly switched automatically.

6. The apparatus (1) according to any of claims 3 to 5, comprising a device (29b, 19b) for keeping said delay device (2) in the second mode after it has been determined that the clock edge (A') of the delayed clock signal (DQS) output by said delay device (2), or of the signal (FB) obtained therefrom, lies within the predetermined time window before the corresponding clock edge (A) of the clock signal (CLK), or of the signal obtained therefrom.

7. An apparatus (1) for utilization with the synchronization of clock signals (CLK), comprising delay device (2) with a variably controllable delay time (t_{var}) that can be decremented or incremented in variably controllable time steps, into which a clock signal (CLK), or a signal obtained therefrom, is input, charged with the variably controllable delay time (t_{var}) that can be decremented or incremented in variably controllable time steps, and output as delayed clock signal (DQS),

wherein additionally a deice (5) is provided for determining whether a clock edge (A') of the delayed clock

signal (DQS) output by said delay device (2), or of a signal (FB) obtained therefrom, lies within a predetermined time window before a corresponding clock edge (A) of the clock signal (CLK), or of the signal obtained therefrom,

and wherein said apparatus (1) is designed and equipped such that, if said device (5) determines that the clock edge (A') of the delayed clock signal (DQS) output by said delay device (2), or of the signal (FB) obtained therefrom, lies within the predetermined time window before the corresponding clock edge (A) of the clock signal (CLK), or of the signal obtained therefrom, the signal delay time (t_{var}) caused by said delay device (2) is decremented or incremented in smaller time steps, and thus more slowly, than prior to the determination,

wherein the duration (Δt) of the time window is chosen as a function of the frequency of the clock signal (CLK) determined by a frequency determination device.

8. A clock signal synchronizing method, comprising the step of:

- charging a clock signal (CLK) or a signal obtained therefrom with a variably controllable delay time (t_{var}), so that a delayed clock signal (DQS) is obtained,

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the method additionally comprises the step of:

- determining whether a clock edge (A') of the delayed clock signal (DQS), or of a signal (FB) obtained therefrom, lies within a predetermined time window before a corresponding clock edge (A) of the clock signal (CLK), or of the signal obtained therefrom.